

CLAIM AMENDMENT:

Please amend claims 17, 22, 23 and 25 and cancel claims 21 and 24.

Claims 1-16 (canceled)

Claim 17 (currently amended): A method of manufacturing a semiconductor device, comprising:

preparing an SOI substrate;

forming a metal layer on the SOI substrate;

annealing the metal layer at a first temperature, which is effective in converting the metal layer into a first silicide layer;

forming an insulating layer on the first silicide layer; and

forming a hole from a surface of the insulating layer until a part of the first silicide layer is exposed; and

annealing the first silicide layer at a second temperature, which is effective in converting the first silicide layer into a second silicide layer by a rapid thermal annealing process wherein the second temperature is higher than the first temperature.

Claim 18 (previously presented): A method as claimed in claim 17 wherein the metal layer includes cobalt.

Claim 19 (previously presented): A method as claimed in claim 18 wherein the first silicide layer includes CoSi.

Claim 20 (previously presented): A method as claimed in claim 19 wherein the second silicide layer includes CoSi_2 .

Claim 21 (cancelled).

Claim 22 (currently amended): A method as claimed in claim ~~[[21]]~~ 17 wherein ~~the rapid thermal annealing~~ the metal layer is carried out at a temperature in a range between about 450 °C and about 550 °C.

Claim 23 (currently amended): A method as claimed in claim ~~[[22]]~~ 17 wherein ~~the rapid thermal annealing~~ the metal layer is carried out at a temperature of about 550 °C for about 30 seconds.

Claim 24 (cancelled).

Claim 25 (currently amended): A method as claimed in claim ~~[[24]]~~ 17 wherein the rapid thermal annealing is carried out at a temperature of about 800 °C.

Claim 26 (previously presented): A method as claimed in claim 17 wherein the SOI substrate has a thickness of 50nm or less.

Claim 27 (previously presented): A method as claimed in claim 17 wherein the hole has a diameter of 0.1 μ m or less.

Claim 28 (previously presented): A method as claimed in claim 17 wherein a time period of annealing the metal layer is shorter than that of annealing the first silicide layer.

Claim 29 (previously presented): A method as claimed in claim 17 wherein a difference between the first temperature and the second temperature is 350 °C or less.

Claim 30 (previously presented): A method as claimed in claim 17 wherein a resistance value of the first silicide layer is higher than that of the second silicide layer.